Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-2. (Cancelled).

3. (Previously presented) A unit as in claim 30 which includes additional circuits to evaluate the received synchronizing signal and, responsive thereto, to determine if an additional message is expected.

4. (Previously presented) A unit as in claim 3 which includes further circuitry to extend the active mode and to acquire and respond to any expected additional message.

5. (Original) A unit as in claim 3 where the control circuitry comprises, at least in part, a processor and executable instructions.

6. (Original) A unit as in claim 5 which includes timer circuitry, coupled to the processor, for initiating the periodic, limited duration active mode.

7. (Previously presented) A unit as in claim 5 which includes executable instructions for at least receiving data using a different protocol than a protocol exhibited by the synchronizing signal.

8. (Previously presented) A unit as in claim 5 which includes executable instructions for transmitting data with a different protocol than a protocol of the received synchronizing signal.

9. (Original) A unit as in claim 7 which includes executable instructions that sense and decode multiple data signals received from multiple sources substantially simultaneously.

10. (Previously presented) A unit as in claim 9 where the sense and decode process comprises bit arbitration.

11. (Cancelled).

12. (Previously presented) A method as in claim 32 which includes evaluating multiple simultaneously received data signals and discerning one from another.

13. (Original) A method as in claim 12 which includes minimizing energy requirements at a plurality of synchronizing signal receiving locations between such signals.

14-15. (Cancelled).

16. (Previously presented) A system as in claim 33 where at least one of the second device or the third device includes a battery.

17. (Previously presented) A system as in claim 33 where the synchronization signal is transmitted periodically with a predetermined timing.

18. (Previously presented) A system as in claim 33 where the synchronization signal includes at least one of RF frequencies, optical frequencies or sonic frequencies.

19. (Previously presented) A system as in claim 33 where the synchronizing function includes transmitting a signal representative of a detector state.

20. (Original) A system as in claim 18 where a detector state comprises at least one of an alarm, trouble, voltage, input, or sensor condition.

21. (Original) A system as in claim 18 where the first device receives the transmitted signal.

22. (Original) A system as in claim 18 wherein the said transmitting of a signal includes at least in part a frequency that is the same as the synchronization signal frequency.

23. (Previously presented) A system as in claim 33 where the synchronization signal includes variable frequencies.

24. (Previously presented) A system as in claim 33 which includes a plurality of devices receiving the wireless synchronization signal.

25. (Original) A system as in claim 24 where members of the plurality each include circuitry to transmit data signals at different offsets from the synchronizing signal in response to at least one of, a substantially random number, or, a unique device identifier.

26-29. (Cancelled).

30. (Currently amended) An electrical unit having:

a wireless communications port;

a transceiver coupled to the port; and

control circuitry coupled to the transceiver, the control circuitry and transceiver have, at least, an inactive mode interrupted by an intermittent, limited duration higher power active mode, the control circuitry including circuitry to monitor the port for receipt of a wireless synchronization signal, and responsive thereto to establish a predetermined time offset from the wireless synchronizing signal and only a receiver portion of the transceiver to enter the active mode at a time interval, corresponding to the offset, prior to receipt of subsequent wireless synchronizing signals and to receive other incoming signals with the control circuitry responding to an incoming signal requesting information by causing a transmitter portion of the transceiver to enter the active mode and transmitting requested information using at least one byte of information having a plurality of bits via the transceiver and where the control circuitry

simultaneously monitors signals received from the transceiver and by checking that the received signal is the same as the transmitted signal determines for each bit of the plurality of bits that a higher priority message is being received and responsive to that determination terminates the transmission before completion of the byte.

31. (Previously presented) A unit as in claim 30 where the control circuitry subsequent to terminating the transmission, restarts transmitting the requested information via the transceiver and where the control circuitry again simultaneously monitors signals received from the transceiver to determine if a higher priority message is being received.

32. (Currently amended) A method which comprises:

transmitting a sequence of common wireless synchronizing signals;

prior to receiving a synchronizing signal, a receiver portion of a transceiver under control of an internal clock entering an active mode to receive and evaluate the synchronizing signal, and responsive thereto while in the active mode a transmitter portion of the transceiver entering the active mode, the transceiver receiving an information request ~~or~~ and transmitting ~~data~~ a response to the information request based upon its internal state condition;

the transceiver continuously remaining in the active mode for a period of time at least until no further bytes of data each having a plurality of bits is being received or transmitted and which includes conducting bit arbitration while transmitting ~~data and;~~ data;

comparing each transmitted bit of the information response with a simultaneously received bit; and

terminating the transmission before completion of the byte upon detecting that the received signal is not the same as the transmitted signal.

33. (Currently amended) A communication system having at least three devices that can wirelessly transmit and receive signals comprising:

a first device that transmits a sequence of wireless, common, synchronization signals;

at least a second device receiving the wireless synchronization signals, the second device synchronizes functions to the synchronization signals under control of an internal clock such that

energy consumption of a receiver of the second device is increased for a period of time before, during and immediately after each synchronization signal;

at least a third device receiving the wireless synchronization signals, the third device synchronizes functions to the synchronization signals under control of an internal clock such that the energy consumption of a receiver of the third device is increased for a period of time before, during and immediately after each synchronization signal, where the second device receives a wireless signal including an information request and transmits a response to the information request based upon its internal state condition, said response having at least one byte of information with a plurality of bits ~~from~~ with said transmitted response of the second device received by the third device and the third device receives a wireless signal including an information request and transmits a response to the information request based upon its internal state condition, said response having at least one byte of information with a plurality of bits ~~from~~, said transmitted response of the third device being received by the second device and where energy consumption of transmitters of each of the second and third devices is increased and each of the second and third devices carries out a bit arbitration process while wirelessly transmitting signals at the same time, said bit arbitration including comparing each bit of the transmitted responses with each received bit; and

the second or third device terminating transmission before completion of the byte upon detecting that the received signal is not the same as the transmitted signal.